In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. to 4. (Canceled)

5. (Previously Presented) A digital signal processing system, comprising:

a plurality of processor subsystems that each include:

at least one memory device; and

a memory bus multiplexer coupled to each of said at least one memory device by a subsystem memory bus; and

a direct memory access (DMA) controller,

an input/output peripheral coupled to the subsystem memory bus,

wherein each of the DMA controllers is coupled to each of said memory bus multiplexers of each of said plurality of processor subsystems and is configured to access each of said memory devices of each of said plurality of processor subsystems via the corresponding subsystem memory bus, and

wherein each of the DMA controllers is configured to access each of the peripherals via the corresponding subsystem memory bus.

6. (Previously Presented) A digital signal processing system, comprising:

a plurality of processor subsystems that each include:

at least one memory device; and

a memory bus multiplexer coupled to each of said at least one memory device by a subsystem memory bus; and

a direct memory access (DMA) controller,

a host port interface (HPI) unit coupled to the memory bus multiplexer and configured to access the memory device via the subsystem memory bus; and

a remote access multiplexer coupled between the memory bus multiplexer and all DMA controllers outside the processor subsystem, wherein the remote access multiplexer is further coupled between the memory bus multiplexer and all HPI units outside the processor subsystem,

wherein each of the DMA controllers is coupled to each of said memory bus multiplexers of each of said plurality of processor subsystems and is configured to access each of said memory devices of each of said plurality of processor subsystems via the corresponding subsystem memory bus;

wherein each of the HPI units is coupled to each of the memory bus multiplexers and is configured to access each of the memory devices via the corresponding subsystem memory bus wherein each of the HPI units is coupled to each of the memory bus multiplexers and is configured to access each of the memory devices via the corresponding subsystem memory bus; and

wherein the memory bus multiplexer is configured to couple to the memory bus at any one time exactly one of the HPI unit, the DMA controller, and the remote access multiplexer.

7. (Original) The system of claim 6, wherein each of the plurality of processor subsystems further includes:

a remote access arbiter coupled to the remote access multiplexer and configured to set the remote access multiplexer to couple to the memory bus multiplexer at any one time exactly one of the HPI units and DMA controllers outside the processor subsystem.

8. (Original) The system of claim 6, wherein each of the plurality of processor subsystems further includes:

a memory bus arbiter coupled to the memory bus multiplexer to arbitrate between access requests received from the HPI unit, the DMA controller, and the remote access multiplexer, wherein said arbitration is performed on a round-robin basis.

9. (Canceled)

10. (Previously Presented) A digital signal processor chip, comprising:

a plurality of memory bus multiplexers, each of the memory bus multiplexers is coupled to one or more corresponding memory devices by a corresponding memory bus;

a plurality of DMA controllers each coupled to each of the plurality of memory bus multiplexers, each of the DMA controllers is configurable to access each of the memory devices via a corresponding one of the plurality of memory bus multiplexers;

a plurality of memory bus arbiters each coupled to a respective memory bus multiplexer, wherein each of the plurality of memory bus arbiters is configured to set their respective memory bus multiplexers to grant access

to the corresponding memory bus in response to one or more access requests from the plurality of DMA controllers;

a plurality of host port interface (HPI) units each coupled to each of the plurality of memory bus multiplexers, and each configured to access each of the memory devices via a corresponding one of the plurality of memory bus multiplexers; and

a plurality of memory bus arbiters each coupled to a respective memory bus multiplexer, and each configured to arbitrate between a local DMA controller, a local HPI unit, and a remote access multiplexer for access to a memory bus.

11 and 12. (Canceled)

13. (Previously Presented) The chip of claim 10, further comprising a plurality of memory bus arbiters each coupled to a respective memory bus multiplexer, wherein each of the plurality of memory bus arbiters is configured to set their respective memory bus multiplexers to grant access to the corresponding memory bus in response to one or more access requests from the plurality of DMA controllers.

14. (Original) The chip of claim 13, wherein the arbiters are further configured to resolve conflicts on a round-robin priority basis and grant only one access request at a time.

15 and 16. (Canceled)

17. (Original) A multi-core digital signal processor, comprising:

a first processor subsystem that includes:

a first processor core;
a first memory device coupled to the first processor core by a first instruction bus;
a first memory bus multiplexer coupled to the first memory device by a first memory bus;
a first DMA controller coupled to the first memory bus multiplexer and configured to control the first memory bus to access the first memory device;
a first HPI unit coupled to the first memory bus multiplexer and configured to control the first memory bus to access the first memory device; and
a first remote access multiplexer coupled to the first memory bus multiplexer; and

a second processor subsystem that includes:
a second processor core;
a second memory device coupled to the second processor core by a second instruction bus;
a second memory bus multiplexer coupled to the second memory device by a second memory bus;
a second DMA controller coupled to the second memory bus multiplexer and configured to control the second memory bus to access the second memory device;
a second HPI unit coupled to the second memory bus multiplexer and configured to control the second memory bus to access the second memory device; and
a second remote access multiplexer coupled to the second memory bus multiplexer,

wherein the first DMA controller is coupled to the second remote access multiplexer and is configured to control the second memory bus to access the second memory device, and

wherein the second DMA controller is coupled to the first remote access multiplexer and is configured to control the first memory bus to access the first memory device.

18. (Original) The processor of claim 17, wherein the first HPI unit is coupled to the second remote access multiplexer and is configured to control the second memory bus to access the second memory device, and wherein the second HPI unit is coupled to the first remote access multiplexer and is configured to control the first memory bus to access the first memory device.

19. (Original) The processor of claim 17, further comprising a first arbiter coupled to the first memory bus multiplexer and configured to arbitrate between the first DMA controller, the first HPI unit, and the first remote access multiplexer for control of the first memory bus.